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Electronically Transparent Graphene Barriers against Unwanted Doping of Silicon

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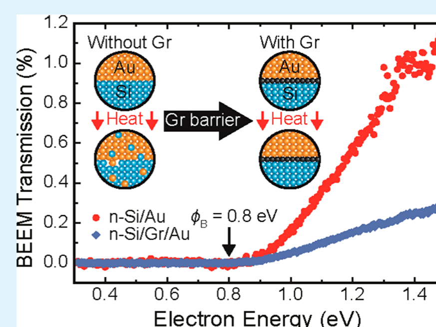
Supporting Information

ABSTRACT: Diffusion barriers prevent materials from intermixing (e.g., undesired doping) in electronic devices. Most diffusion barrier materials are often very specific for a certain combination of materials and/or change the energetics of the interface because they are insulating or add to the contact resistances. This paper presents graphene (Gr) as an electronically transparent, without adding significant resistance to the interface, diffusion barrier in metal/semiconductor devices, where Gr prevents Au and Cu from diffusion into the Si, and unintentionally dope the Si. We studied the electronic properties of the *n*-Si(111)/Gr/M Schottky barriers (with and without Gr and M = Au or Cu) by $I(V)$ measurements and at the nanoscale by ballistic electron emission spectroscopy (BEEM). The layer of Gr does not change the Schottky barrier of these junctions. The Gr barrier was stable at 300 °C for 1 h and prevented the diffusion of Cu into *n*-Si(111) and the formation of Cu_3Si. Thus, we conclude that the Gr is mechanically and chemically stable enough to withstand the harsh fabrication methods typically encountered in clean room processes (e.g., deposition of metals in high vacuum conditions at high temperatures), it is electronically transparent (it does not change the energetics of the Si/Au or Si/Cu Schottky barriers), and effectively prevented diffusion of the Cu or Au into the Si at elevated temperatures and vice versa.



KEYWORDS: *graphene, diffusion barrier, BEEM, copper, gold, silicon, electronically transparent*

INTRODUCTION

Controlling the properties of metal−semiconductor interfaces is important because they determine whether, for instance, metal−semiconductor contacts are ohmic or not, or control contact resistance. Diffusion of metals into Si may cause unwanted doping and the formation of deep level traps.[1,2] Protective layers that minimize interfacial diffusion in general change the electronic properties of the interfaces they protect.[3] For instance, in microelectronics Cu, W, or Al, diffusion into Si is minimized by using TaN or TiN barriers,[4−8] which are more resistive than the typical interconnect metals, resulting in an increase of power consumption and increased resistive-capacitance delay.[9] In commercial Si-based solar cells, diffusion barriers are avoided by simply using expensive Ag top-electrodes because Ag diffuses slowly into Si relative to the lifetime of the solar cells.[10,11] An "ideal" barrier should fulfill three requirements: the barrier must be (i) impermeable to metal atoms/ions, (ii) mechanically and thermally stable during the fabrication conditions (high vacuum and temperatures (typically up to 1000 °C)), and (iii) electronically transparent (does not affect the electronic properties of the interface it protects).

We propose to use graphene as a protection barrier against metal diffusion for the following five reasons. (i) It is impermeable to gases[12] and metal atoms.[13] (ii) It has no band gap[14] and forms ohmic contact with most metals. (iii) It is atomically thin and electrons tunnel through the graphene barrier layer easily.[15,16] (iv) It has great mechanical stability with a Young's modulus of 1 TPa.[17] (v) It is chemically stable, has high thermal conductivity[18] and it can withstand thermal stressing up to 400 °C in air,[19] and estimated up to 2300 °C in vacuum.[20] Here we describe the use of graphene (Gr) as a protective barrier for hydrogen passivated *n*-Si(111)/Cu and *n*-Si/(111)Au structures. We found that the barrier height of

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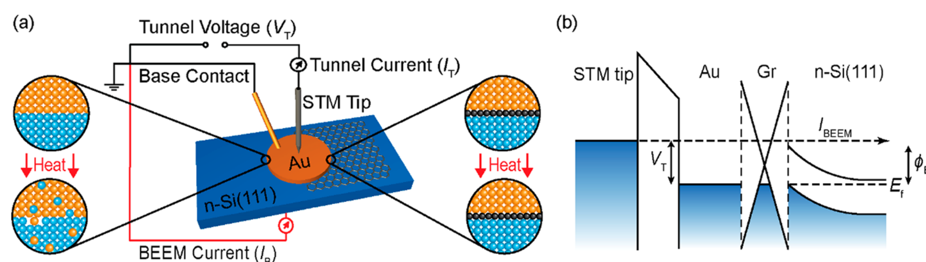

Figure 1. (a) Schematic of the STM/BEEM apparatus and the n-Si(111)/Gr/Au device with and without the Gr protective barrier and the corresponding energy level diagram (b), the base contact in (a) serves as a common contact for ground in BEEM measurements or to apply a bias in $I(V)$ measurements.

these Schottky barriers were not altered by the presence of the Gr layer, no metal atoms diffused into the Si layer (within detection limits), and the Gr protective barrier withstood the harsh fabrication conditions. From this experiment, we conclude that Gr is an electronically transparent protective barrier and blocks unwanted doping at the atomic level.

Often the fabrication of a well-defined interface is troublesome because during the fabrication steps (that often require high temperatures and high-vacuum conditions, etching, or chemical and mechanical cleaning steps) the materials at the interface may be damaged, or diffuse into one and another.[3] Figure 1a shows schematically a damaged interface where one material diffused into the other and an "ideal" interface where diffusion is avoided by a protective barrier. These protection layers often add to the contact resistance (and higher power consumption),[9] and change the interface energetics, which impact device behavior. Often these protection layers have been optimized for certain specific applications.[4−8] TaN,[4] Ta,[7] or bilayer TaN/Ta[8] barriers prevent the diffusion of Cu into Si and low κ dielectrics for Cu metallization, or TiN[5,6] for W/Al metallization. Existing protective barriers change the electronic properties of the interface due to the differences in work functions of the different materials. For instance, TaN forms a Schottky barrier of 0.48 eV with n-type silicon and 0.68 eV with p-type silicon,[21] TiN forms a Schottky barrier of 0.55 eV with n-type silicon and 0.57 eV with p-type silicon.[22] These differences in the Schottky barrier heights result in drastic changes to the energetics of the interfaces complicating the design and fabrication process.

Ag, Cu, and Au are widely used as interconnects in electronic devices, as they have the highest electrical conductivities amongst metals.[23] Except for Ag, which does not diffuse significantly into Si relative to the lifetime of the devices at low temperatures,[10,11,24] Cu and Au diffuses readily into Si: the interstitial hopping energy of Cu is only 0.18 eV and the diffusion coefficient of Cu in Si is 2.84×10^{-7} cm^2 s^{-1} at 300 K,[25] which is 4 orders of magnitude higher than that of Au[26] and 7 orders of magnitude higher than that for Ag.[11] This means that at 300 K, Cu can diffuse across the whole thickness of a standard 500−600 μm Si wafer in a few hours. The diffusion barrier for the current 22 nm technology is about 3 nm thick TaN, which prevents diffusion of Cu into Si.[27] The drive for device miniaturization of microelectronic components also includes reducing the thickness of the protective barriers to minimize resistance and power loses.[9] Reducing the resistivity by reducing the thickness is an obvious strategy to reducing resistances, but the barrier performance decreases with decreasing thickness. The resistivity of TaN is about a factor of 10 to 100 higher than Cu, depending on the deposition conditions, stoichiometry, and phases.[28] Although subnanometer TaN barriers have been demonstrated by atomic layer deposition (ALD),[29] these films tend to be highly resistive, expensive, and difficult to scale up, and thus are not ideal for use in interconnects. Hence, a monatomic thin layer that effectively blocks diffusion without adding significant resistance is required to further down-size microelectronics.[30,31]

This paper describes the properties of the buried n-Si(111)/Gr/metal interfaces using ballistic electron emission microscopy (BEEM) and current−voltage $I(V)$ measurements. Figure 1 shows the energy level diagram and illustrates how BEEM can be used to determine the Schottky interface heights of a buried interface with nanometer spatial resolution.[32,33] Ballistic electrons emitted from an STM tip probe the buried Schottky interface of a metal/semiconductor interface. In BEEM experiments, electrons are injected into a thin metal base, i.e., the thin (here 15 nm) gold layer in Figure 1a, from the STM tip by applying a negative tip bias, while the metal base and the semiconductor substrate are grounded. A portion of these electrons are not scattered, the ballistic electrons, as they travel through the metal base to reach the metal−semiconductor Schottky interface and subsequently they are collected as the BEEM current at the backside of the semiconductor if they have enough energy to overcome the Schottky barrier (ϕ_B) and fulfill the momentum conservation rules.[32,33] The BEEM current is a function of the bias applied between the tip and the metal base. Because the lateral position of the STM tip can be controlled with atomic scale precision, the BEEM response can be mapped with typically nanometer scale resolution.[33]

Graphene has been used as protection barriers before in oxidation resistant coatings,[34] molecular electronics,[35] metal diffusion barriers,[13,30,31] and other applications.[36] Nguyen et al.[30] reported using trilayer graphene as a Cu diffusion barrier for applications in microelectronics and Hong et al.[31] reported using monolayer graphene as a Cu diffusion barrier. However, the electronic behavior of the graphene barrier layer in semiconductor/graphene/metal devices have not been characterized thoroughly. Here we use BEEM and $I(V)$ measurements to show that Gr is a promising material to protect barriers at the nanoscale while introducing negligible resistance and does not change the energetics of the interface. Our findings are important because graphene can be used to prevent incompatible materials from diffusing into one another without changing the electrical properties of the interface (electronically transparent). We postulate that the electronic transparency of the graphene barrier is important in applications where unwanted doping must be avoided without introducing significant resistance.[37−40]

EXPERIMENTAL DETAILS

Fabrication of the Si/Gr/Metal Structures. The *n*-type silicon (111) wafers (1−10 Ω, phosphorus doped) were purchased from Syst Integration, diced into 6 × 6 mm, and used as the semiconductor substrate. Prior to Schottky metal or graphene deposition, the silicon wafers were cleaned by 1 min sonication in acetone (CMOS grade, J.T. Baker) and isopropyl alcohol (CMOS grade, J.T. Baker), to remove organic contaminants followed by a brief etch in buffered hydrofluoric acid (Honeywell (7:1) Buffered Oxide Etchant) for 60 s to remove the native SiO_2 layer and to form a hydrogen passivated surface.[41]

Monolayer graphene on Cu (Bluestone Global Tech) was transferred using a previously reported wet transfer process.[42] We spin coated a layer of PMMA of ∼200 nm (A4 495k, MicroChem Corp; at 2500 rpm for 40 s) on Gr on Cu followed by a 80 °C bake for 15 min to remove residual solvents. The PMMA film functions as the support in the transfer process. The graphene on the backside of the copper foil was removed in O_2 plasma (50 W, 15 min, 0.5 mbar). The 25 μm thick Cu substrate was then etched away by floating the Cu/Gr/PMMA stack in an aqueous solution of ammonium persulfate (Alfa Aesar; 10 wt % solution in deionized water) for 3 h. The Gr/PMMA stack was washed by repeated transfer onto copious amounts (5 × 1 L) of deionized water using an oxygen plasma treated Si wafer before transferring onto a freshly prepared hydrogen passivated silicon surface and dried naturally in the clean room environment.

Metal deposition was carried out in a thermal evaporator (R-DEC co. UNS021) with $<5 \times 10^{-7}$ mbar base pressure using Au (99.99%; Advent Research Materials) or Cu (99.999%; Advent Research Materials) in a tungsten boat (Kurt J. Lesker). We deposited a layer of 15 nm of Au, or 100 nm of Cu, at 0.2 Å/s, monitored using a quartz crystal balance (Inficon XTM/2), through a shadow mask containing a 5 × 5 array of 0.5 mm diameter circular holes in a 100 μm thick stainless steel sheet. The device area was determined by scratching the graphene using a sharp tweezer between the 0.5 mm diameter Au or Cu dots to prevent leakage currents due to the high conductivity of graphene in the *xy*-plane.

Electrical Characterization. The $I(V)$ and STM/BEEM[32,33] measurements were carried out with a home-built STM/BEEM setup (Figure 1a); the details of this setup have been described elsewhere.[43] Briefly, a thin gold wire (50 μm) held by a high precision manipulator (Kleindiek Nanotechnik) was used to ground the Au base electrode for BEEM measurements or to apply a bias during $I(V)$ measurements. An ohmic back contact, made by scratching the native oxide layer and depositing Ag (99.999%; Advent Research Materials) or eutectic Ga−In (Sigma-Aldrich), to the semiconductor was connected to a high gain amplifier (FEMTO DHPCA-100) and used as a current collector for BEEM measurements or as the drain in $I(V)$ measurements. The STM/BEEM measurements were all conducted in air and at ambient temperature using mechanically cut Pt−Ir tips on an Agilent STM head and controlled with a Nanonis STM controller.[43] Thermal stressing of the *n*-Si(111)/Cu device was carried out in a high vacuum chamber ($<5 \times 10^{-7}$ mbar) equipped with a feedback controlled sample stage heater. The sample temperature was raised slowly (2.5 °C/min) from room temperature to the desired temperature, holding for 1 h, and then cooled to room temperature by switching off the heater in the vacuum chamber. The $I(V)$ measurements were carried out in a Materials Development Corp (MDC) CV−IV Measuring System from −0.5 to 1 V with a step size of 7.5 mV and 0.1 s hold time.

Suspended Graphene. We fabricated an array of holes with a diameter of 100 nm by electron-beam lithography (Elionix ELS-7000) and reactive ion etching (RIE) (Plasmalab 80, Oxford) in a 100 nm thick Si_3N_4 membrane following a previously published procedure.[44] Briefly, a 170 nm thick ZEP-520A resist was spin-coated onto a 100 nm thick Si_3N_4 membrane substrate and the material was baked at 180 °C for 2 min. Designed patterns (array of 100 nm diameter circles) were exposed at a dose of 300 μC/cm^2 by using an electron beam with an acceleration voltage of 100 kV and beam current of 50 pA. The exposed samples were developed in *o*-xylene for 30 s and rinsed in isopropyl alcohol (IPA) for 20 s. The resist patterns were transferred to the Si_3N_4 membrane layer by RIE in a mixture of CHF_3 (55 sccm) and O_2 (5s sccm) at 0.1 mbar at a power of 175 W for 3 min. The resist was removed in microposit 1165 remover (MicroChem Corp), and the substrates were rinsed with IPA and deionized water and blown dry with nitrogen gas. Onto these holes we transferred Gr followed by thermal deposition of Au (30 nm) using procedures described above. We imaged the structures by SEM (Elionix ESM-9000) using an acceleration voltage of 5 kV for Si_3N_4 to reduce charging effects and 30 kV when coated with Au.

Raman and Atomic Force Microscopy. We characterized graphene using a commercial Witec alpha 300R Raman system with a 532 nm laser (2.33 eV) excitation source. We kept the laser power below 3 mW to avoid laser-induced damage to graphene.[45] A 100× objective lens with a numerical aperture (N.A.) of 0.90 was used to focus the laser spot to about 1 μm in diameter during the Raman measurements. Typical integration time for spectrum acquisition is 5 s for graphene on SiO_2 (280 nm) and 10 s for graphene on Si(111)-H surfaces. Atomic force microscopy images of graphene were recorded in tapping mode (Bruker Dimension Fastscan) using FastScan-A probes (resonant frequency, 1.4 MHz; force constant, 18 N/m).

X-ray Diffraction. We characterized Cu_3Si formation in *n*-Si(111)/Cu devices using a commercial Bruker D8 general area detector diffraction system (GAADS) equipped with a two-dimensional (2D) detector and Cu Kα radiation (λ = 0.154 nm). We recorded the Debye diffraction pattern using the 2D detector from 2θ angle (*x*-axis) of 20° to 85° and integrated the signal over the sample tilt angle χ (*y*-axis). The strong Si(111) substrate peak at 28° is avoided in the scan to prevent detector overloading.

RESULTS AND DISCUSSION

Fabrication. We fabricated *n*-Si(111)/Gr/Au devices by transferring Gr using a wet transfer process onto hydrogen passivated Si(111) using well-established methods[42] followed by Au deposition. As graphene is not visible by the eye on hydrogen passivated Si substrates,[46] we used optical microscopy to characterize the quality of the Gr from the same batch of Cu/Gr by transferring graphene on 280 nm SiO_2 substrates and measured atomic force microscopy (AFM), and Raman spectroscopy on both 280 nm SiO_2 and hydrogen passivated substrates. Figure 2 shows the results from which we make the following observations. (i) The optical micrographs show that the entire Si surface was covered with a Gr layer (with some PMMA residues)[47] and a few islands of bilayer and multilayer Gr, but no cracks were visible. (ii) The AFM images show typical defects such as PMMA residues, wrinkles, and folds, but no cracks. (iii) The Raman spectra show that the ratio of I_{2D}/I_G is ∼2 and the width of the $2D_{monolayer}$ peak is ∼27 cm^{-1} for monolayer graphene, and the I_{2D}/I_G ratio is ∼0.9 and the width of the $2D_{bilayer}$ peak is about ∼46 cm^{-1} for bilayer graphene.[45] The Raman spectra show a small D peak (about 10 times smaller in intensity that the G peak), which is associated with islands of bilayer graphene. From these data, we conclude that we successfully transferred continuous films of Gr similar in quality as previously reported layers.[45,48]

Electronic Properties. Figure 3 shows the $I(V)$ measurements and the ballistic electron emission spectroscopy (BEES) plots[49] of the *n*-Si(111)/Au and the *n*-Si(111)/Gr/Au devices both with 15 nm of Au. We fitted the $I(V)$ curves (forward bias; solid black lines in Figure 3a) to the simplified thermionic emission model (see the Supporting Information) to determine the Schottky barrier height (ϕ_B) and ideality factor (n) as follows.[2]

$$I \approx \left[AA^{**}T^2 \exp\left(\frac{-q\phi_B}{k_B T}\right)\right]\left[\exp\left(\frac{qV_D}{nk_B T}\right)\right] \quad (1)$$

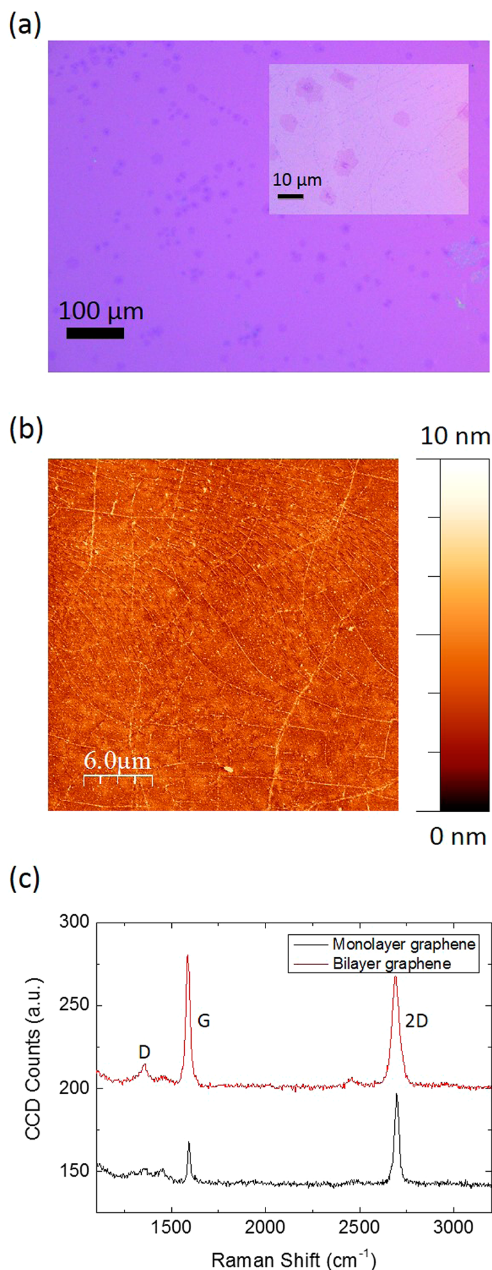

Figure 2. (a) Optical micrographs of Gr on 280 nm SiO_2, (b) AFM images of Gr on *n*-Si(111)-H, and (c) Raman spectra recorded on Gr on *n*-Si(111)-H on an area with monolayer and bilayer graphene.

where q is the electric charge (=1.602 × 10^{-19} C), V_D the voltage applied across the diode, k_B the Boltzmann constant (=1.381× 10^{-23} m^2 kg s^{-2} K^{-1}), T the absolute temperature, A the area of the diode, A^{**} (=1.12 × 10^6 A m^{-2} K^{-2}) the effective Richardson constant of *n*-type Si, and ϕ_B the Schottky barrier height. Fitting the slope of the forward biased $I(V)$ curve in the region of $3k_BT < V < 5k_BT$ gives n, and the intercept of the curve with the y-axis gives the value of ϕ_B (eq 1). We obtained ϕ_B = 0.80 and 0.78 eV for the devices without (with n = 1.08) and with a layer of Gr (with n = 1.20), respectively, similar to previously reported values.[50] From these results, we conclude that on the macroscopic scale, the presence of Gr does not significantly change the electronic properties of the *n*-Si(111)/Au Schottky interface.

Figure 3b shows the BEEM spectra that were obtained as follows. We normalized the transmission of the interface by taking the ratio of the BEEM current (I_{BEEM}), the current that flows through the Schottky interface (between the Au metal base and the *n*-Si(111) substrate), and the tunnel current (I_{tunnel}), the current that flows between the STM tip and the grounded Au metal base (Figure 1). We plotted this ratio vs the electron energy (eV), which is the bias between the tip and the base (V_T). To this so-called BEES spectrum, we fitted the Bell–Kaiser model[33] (eq 2) to determine the local value of ϕ_B (with a spatial resolution of ∼1 nm^2) and the transmission attenuation factor (R). Noisy data that falls below the statistical goodness of fit value of 0.8 were rejected (typically the noisy data come from instrumental noise). We repeated this procedure 900 times over an area of 256 × 256 nm^2 and plotted the results in a 2D graph of R vs ϕ_B (Figure 3c,d), which serves as a unique "BEES fingerprint" of the interface.[49]

$$\frac{I_{BEEM}}{I_{tunnel}} = R\frac{(eV - \phi_B)^2}{eV} \tag{2}$$

We found that the nanoscopic values of $\phi_{B,BEEM,n\text{-}Si(111)/Au}$ = 0.80 ± 0.01 eV and $\phi_{B,BEEM,n\text{-}Si(111)/Gr/Au}$ = 0.78 ± 0.01 eV obtained in BEEM (Figure 3c,d) are essentialy identical within the thermal broadening limit of $3k_BT$, i.e., the Schottky barrier heights were unchanged by the presence of Gr at the interface. The presence of the layer of Gr is apparent in the factor R: by modifying the *n*-Si(111)/Au interface with Gr, the value of R decreased from 0.05 to 0.01 eV^{-1}. The decrease in R-factor shows that there is no direct contact between gold and silicon due to increased scattering of ballistic electrons at the *n*-Si(111)/Gr/Au interfaces[51] and graphene is essentially "electronically transparent" because it does not change the barrier height of the *n*-Si(111)/Au system.

We explain the behavior of the buried Gr layer as follows. It is well-known that charge transfer can occur between graphene and the surface it is immobilized on.[52] We postulate that the Fermi level of Gr shifts toward that of the Au it interacts with, but that the Schottky-barrier height did not change because the doping level of the *n*-Si(111) was not changed. In other words, we postulate that the Schottky–Mott model applies.[2] By considering the density of states of electrons at the Fermi level of Au (∼10^{22} cm^{-3}), which is several orders of magnitude above the density of states in Gr (Dirac cone linear dispersion of Gr implies that the density of states diminishes close to the intrinsic work function of ∼4.6 eV),[53] the transfer of electrons from Au into Gr will effectively dope Gr and results in Fermi level alignment.[52] Further electron transfer from the *n*-type semiconductor to the Au-doped Gr (causing band bending in the semiconductor) renders Gr electronically transparent and the Schottky barrier height unchanged.[54,55] A similar explanation has been used to explain the behavior of Gr on Au showing significant *p*-doping of graphene, with a Fermi level shift of 0.35–0.4 eV[54] and graphene on Pt(111) showing *p*-doping with a Fermi level shift of 0.30 eV.[56]

Although the Schottky–Mott model does not take into account the semiconductor interface states that may cause Fermi level pinning, we assume that surface states of Si interact with graphene in a similar manner they interact with Au. As the surface states are an intrinsic property of the semiconductor,[57] it was not changed in our experiment and does not affect our overall interpretation of the Schottky barrier.

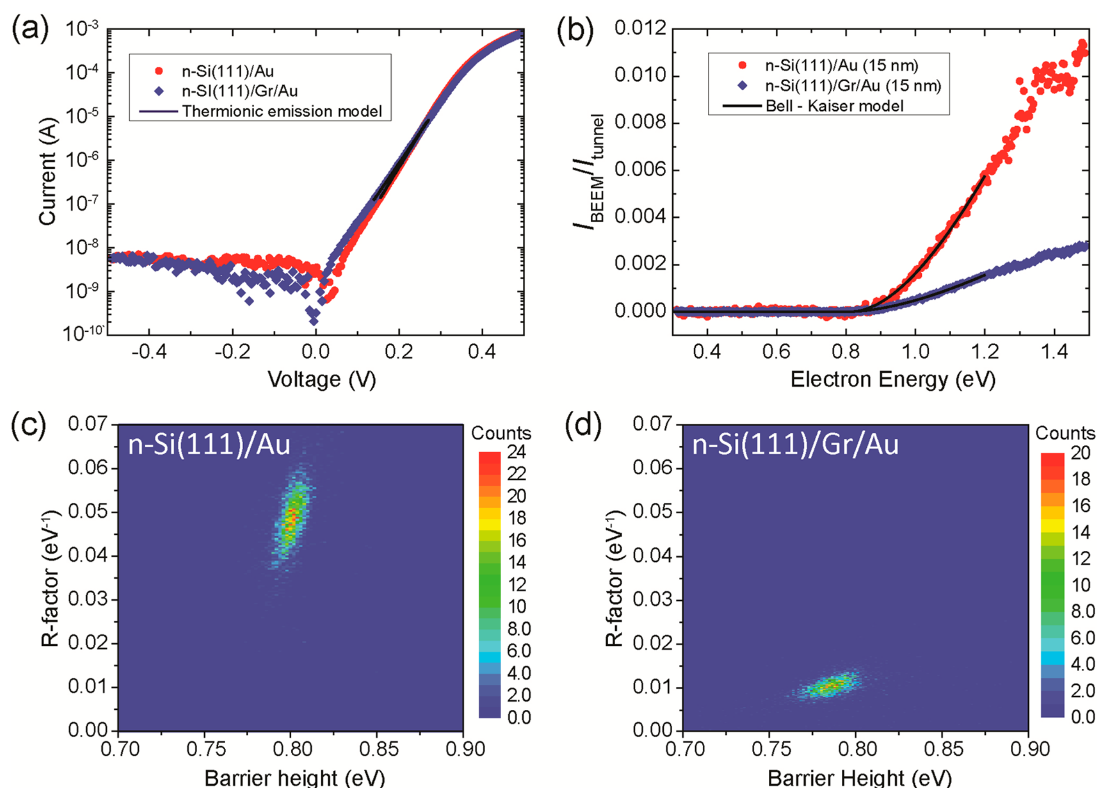

Figure 3. (a) $I(V)$ measurements of the n-Si(111)/Au (15 nm) and the n-Si(111)/Gr/Au (15 nm) interfaces. The solid lines represent fits to the thermionic emission model eq 1. (b) BEEM spectra obtained for the n-Si(111)/Au (15 nm) and the n-Si(111)/Gr/Au (15 nm) interfaces. The solid lines represent fits to Bell–Kaiser model eq 2.[33] Dual parameter BEES plots[49] of R-factor against ϕ_B of (c) n-Si(111)/Au and (d) n-Si(111)/Gr/Au devices.

Mechanical Stability. In addition to electronic transparancy, the mechanical strength of the barrier determines the stability of the protection barrier during the fabrication process of the devices. Measurements of the mechanical strength of graphene by AFM nanoindentation revealed that graphene is the strongest material measured so far, with a Young's modulus of 1 TPa,[17] and that the mechanical strength of polycrystalline CVD graphene is comparable to pristine graphene.[58] Jin et al. and Dulbak et al. reported that sputter deposition induced disorder and damaged graphene,[59,60] therefore it is not a priori known whether Gr can withstand the rough conditions during thermal metal deposition.

To test the mechanical stability of the graphene layer during metal deposition, we deposited metal onto suspended graphene to investigate if the graphene can withstand the impact of the metal atoms and clusters during metal evaporation. By using suspended graphene, we use the worst case scenario where nothing is supporting the graphene layer during metal deposition (Figure 4a). We transferred single layer graphene on an array of holes (20 × 20 μm) with a diameter of 100 nm in silicon nitride (Figure 4c). Subsequently, we deposited Au by thermal evaporation at a rate of 0.2–0.3 Å/s (at a base pressure of <5 × 10^{-7} mbar). Figure 4 shows the scanning electron microscopy (SEM) images of the Gr on the Si_3N_4 membrane before (Figure 4c) and after metal deposition (Figure 4e). As described earlier, some PMMA residues on Gr from the transfer process are still present[47] and are used as markers for locating the same device area after Au deposition (Figure S1; see the Supporting Information) The contrast of the SEM images of the pattern in Si_3N_4 increases because the conductive nature of Gr avoids charging (Figure 4c). Although PMMA residues are

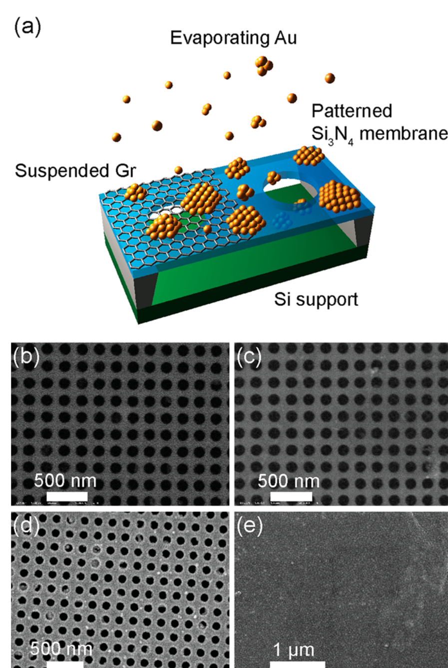

Figure 4. (a) Schematic of the suspended graphene experiment. Au (30 nm) was evaporated onto graphene suspended over 100 nm diameter holes lithographically patterned in silicon nitride. Scanning electron micrographs of the 100 nm diameter holes in Si_3N_4, without (b) and with Gr (c). SEM images after the deposition of 30 nm of gold on the holes without (d) and covered with Gr (e).

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present on the Gr film from the transfer process, we do not expect that they affect the mechanical strength of Gr due to very low stiffness and strength of PMMA.[58]

Figure 4e shows that the metal film is smooth, which indicates that the layer of Gr is not damaged during metal deposition. As a control, we also imaged an area of the membrane that was not covered with graphene (on the same sample) from which we conclude that the metal penetrated the holes (only about 5% of the holes clogged likely because of dust particles or process residues) and that the metal itself did not clog up all the holes. Hence, the suspended graphene is robust enough to withstand the impact from clusters of gold atoms[61,62] during metal deposition and withstands the high temperature differences (melting point of gold is 1064 °C and typical deposition temperatures are about 1800 °C).[61]

Thermal Stability. As mentioned earlier, many fabrication steps require elevated temperatures at which besides Cu diffusion also the formation of Cu_3Si is an issue.[63] To investigate the thermal stability of the junctions, we followed the thermal stability by measuring the $I(V)$ curves as a function of annealing temperature. Figure 5 shows the $I(V)$ measurements of the n-Si(111)/Cu and n-Si(111)/Gr/Cu junctions before and after annealing at 100, 200, and 300 °C for 1 h. We fitted the forward bias current with the thermionic emission model (eq 1) as described above to extract the ϕ_B and n. Plotting the leakage current (I_S) of the n-Si(111)/Cu and n-Si(111)/Gr/Cu junctions at −0.5 V against the annealing temperature (Figure 5c) shows an increase of I_S for the unprotected n-Si(111)/Cu devices, which started to degrade when heated above 100 °C. Remarkably, the value of I_S decreased for n-Si(111)/Gr/Cu devices, suggesting that the device properties improved after thermal stressing.

Table 1 lists the values of the Schottky barrier heights and ideality factors obtained by eq 1 following the same procedure as described above. We also determined the series resistance of the diodes (R_{series}) for n-Si(111)/Cu and n-Si(111)/Gr/Cu devices before and after thermal stressing by using the modified thermionic emission model (eq 3) to include the combination of a resistor with resistance R_{series} and the diode through which the current I flows.[64] The voltage V_D across the diode is expressed in terms of the total voltage drop across the resistor and the diode. Using $V_D = V - IR_{series}$, and for $V_D > 3kT/q$, eq 1 becomes

$$I \approx I_s\left[\exp\left(\frac{q(V - IR_{series})}{nkT}\right)\right] \quad (3)$$

Table 1 shows that R_{series} decreased, but the values of ϕ_B decreased and n increased when we subjected the n-Si(111)/Cu devices to thermal stressing above 200 °C. We attribute the decrease of ϕ_B and increase of n to the formation of Cu_3Si alloy because of interfacial reaction between Cu and Si (see below for details).[62] We attribute the decrease in R_{series} to Si doping by Cu diffusion at low temperature (100 °C) and the formation of the Cu_3Si at elevated temperatures (>200 °C; see below). It has been reported before that Cu_3Si formation in Si nanowires reduces the resistance of Si due to doping[65] and we propose that a similar mechanism exists in our n-Si(111)/Cu devices to decrease R_{series}. The formation of Cu_3Si could also result in an increase in the effective contact area due to the formation of spikes[6] at the interface, resulting in an increase in the currents at both reverse and forward bias.

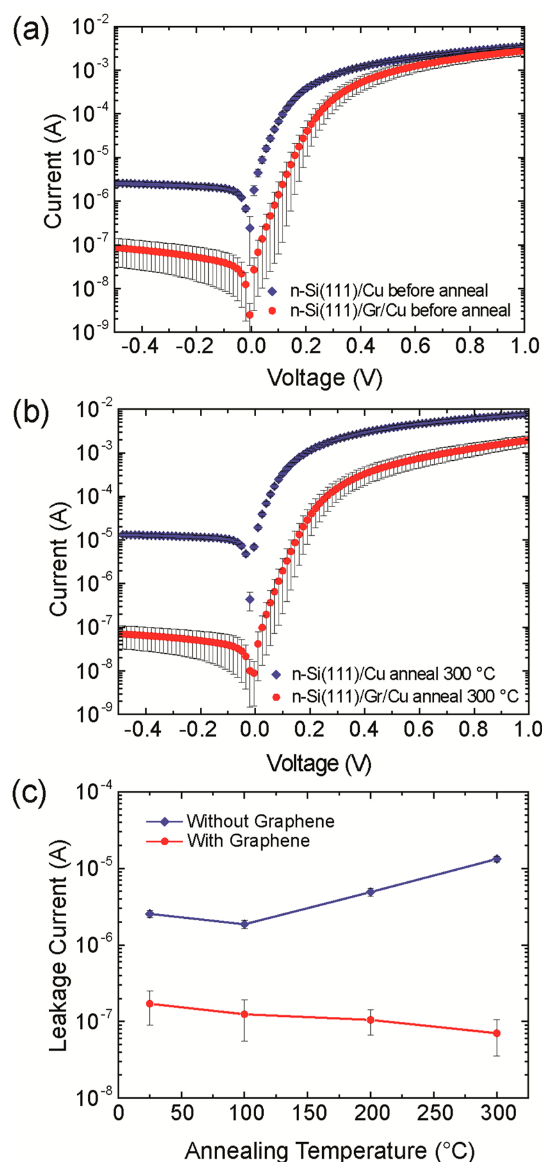

Figure 5. (a) $I(V)$ measurements of n-Si(111)/Cu and n-Si(111)/Gr/Cu before annealing and (b) after annealing at 300 °C for 1 h. (c) Reverse saturation current I_s at −0.5 V plotted against the annealing temperature for Si/Cu and Si/Gr/Cu devices.

For the n-Si(111)/Gr/Cu devices, the values of ϕ_B and n remained unchanged after annealing up to 300 °C for 1h showing that the devices remained intact after thermal stressing. The reverse saturation current of n-Si(111)/Gr/Cu devices decreased, which indicates that these junctions improved in their performance. The decrease of R_{series} could be due to improved contacts of the Gr with the Si and/or Cu layers.

Although the ϕ_B of n-Si(111)/Gr/Cu devices have higher barrier heights than the unprotected n-Si(111)/Cu devices, we explain that due to the high diffusivity of Cu in Si, the as-deposited n-Si(111)/Cu devices are doped by Cu and have a reduced barrier height because of the formation of Cu related defect states at the interface. This effect is also evident in the reduction in ideality factor from n = 1.57 of the n-Si(111)/Cu devices to n = 1.13 of the n-Si(111)/Gr/Cu devices.

Silicide Formation. In the previous section, we inferred that silicides are formed at elevated temperatures. We used

Table 1. Electrical Properties of the *n*-Si(111)/Cu and *n*-Si(111)/Gr/Cu Junctions vs Temperature

	n-Si(111)/Cu			*n*-Si(111)/Gr/Cu		
annealing temperature (°C)	barrier height (eV)	ideality factor *n*	series resistance (Ω)	barrier height (eV)	ideality factor *n*	series resistance (Ω)
RT	0.567 ± 0.004	1.57 ± 0.06	261 ± 17	0.70 ± 0.05	1.13 ± 0.11	546 ± 124
100	0.570 ± 0.010	1.58 ± 0.19	188 ± 60	0.72 ± 0.03	1.08 ± 0.02	500 ± 109
200	0.539 ± 0.003	1.96 ± 0.11	185 ± 14	0.70 ± 0.03	1.11 ± 0.04	286 ± 65
300	0.515 ± 0.002	2.05 ± 0.07	134 ± 16	0.69 ± 0.02	1.14 ± 0.07	311 ± 64

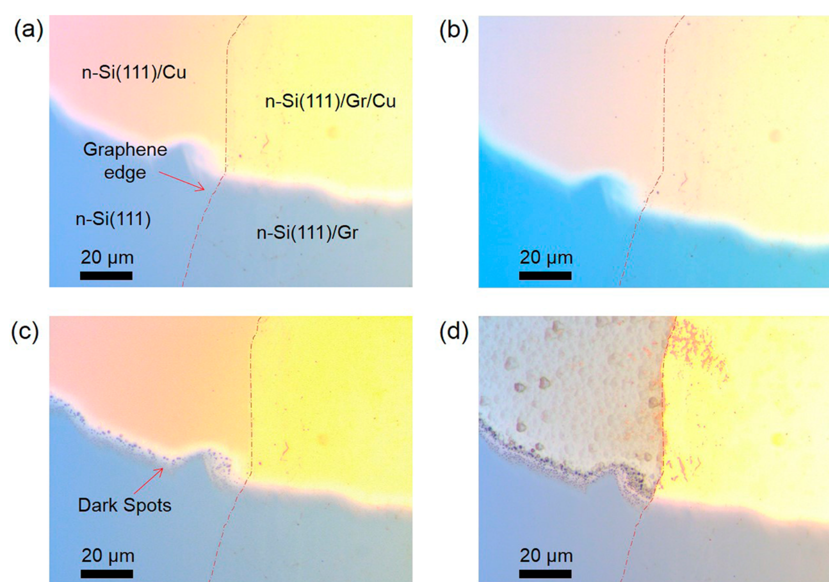

Figure 6. Optical micrographs of a boundary of *n*-Si(111)/Gr/Cu and *n*-Si(111)/Cu devices at room temperature (a), and after thermal stressing in high vacuum for 1 h at 100 °C (b), 200 °C (c), and 300 °C (d).

optical microscopy and X-ray diffraction (XRD) to follow silicide formation. Figures 6 and 7 show the optical images and X-ray diffractograms of the devices before and after thermal stressing, respectively. Figure 6 shows the optical micrographs of the boundary between the protected *n*-Si(111)/Gr/Cu and unprotected *n*-Si(111)/Cu as a function of temperature. Annealing at 200 °C for 1 h results in the appearance of dark spots (Figure 6c) and annealing at 300 °C for 1 h (Figure 6d) results in a complete change in surface morphology. The graphene protected areas remained unchanged over the course of thermal annealing except for some lateral diffusion of Cu_3Si into Cu film in Figure 5d.

To confirm the formation of Cu_3Si, we performed X-ray diffraction (XRD) of the unprotected *n*-Si(111)/Cu and the protected *n*-Si(111)/Cu interfaces. Figure 7 shows the X-ray diffractograms of 2θ against intensity of the as-deposited *n*-Si(111)/Cu and *n*-Si(111)/Gr/Cu devices before and after annealing at 200 and 300 °C for 1 h. The formation of Cu_3Si peaks (red lines, Figure 7) after annealing above 200 °C shows that the interface degraded due to interdiffusion and alloying of Cu and Si. The XRD spectra for protected *n*-Si(111)/Gr/Cu interface showed no alloying even after annealing up to 300 °C for 1 h.

Nguyen et al.[30] and Hong et al.[31] reported using trilayer and monolayer graphene as a Cu diffusion barrier respectively and showed that graphene prevented the diffusion of Cu into Si up to annealing at 700 °C for 30 min. Our results using monolayer graphene supports their conclusion that graphene functions as an effective diffusion barrier for use in Cu metallization and we further show that Gr is an electronically transparent barrier and does not change the energetics of the interface. We did not anneal the *n*-Si(111)/Gr/Cu beyond 300 °C but we expect similar barrier behavior as observed by Hong et al.,[31] as they used a similar CVD graphene.

■ CONCLUSIONS

Here we show that graphene is electronically transparent when sandwiched between silicon and Au or Cu. Both Au and Cu do not penetrate the graphene barrier during the direct evaporation step or by diffusion even during thermal stressing. We studied the *n*-Si(111)/Gr/Au interface by BEEM (~1 nm^2 spatial resolution) and showed that there is no direct contact between *n*-Si(111) and Au at the nanoscale and the *n*-Si(111)/Gr/Au barrier height remains unchanged. Remarkably, thermal stressing at 300 °C for 1 h reduced the contact resistance and lowered the leakage currents across the diodes. In other words, thermal stressing resulted in a measurable improvement of the diode characteristics. In addition, the Gr layer also prevented the formation of silicides. The layer of Gr introduced negligible resistance and is therefore "electronically transparent". Thus, our results show that atomically thin Gr is a promising material to protect interfaces (i) it does not introduce significant resistances, (ii) it is chemically and mechanically stable during the fabrication process, and (iii) it blocks unwanted doping. Currently, we are investigating how the number of Gr layers affect the junction properties.

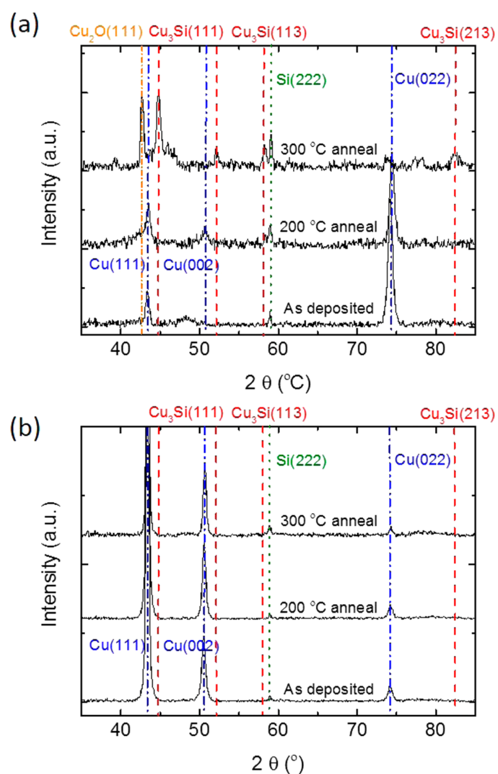

Figure 7. XRD spectra of (a) *n*-Si(111)/Cu before and after annealing at 200 and 300 °C for 1 h showing the formation of Cu_3Si after annealing at 200 °C. (b) *n*-Si(111)/Gr/Cu before and after annealing at 200 and 300 °C.

ASSOCIATED CONTENT

Supporting Information

Derivation of the simplified thermionic emission model (eq 1) and a scanning electron micrograph of the Si_3N_4 membrane with the marked location of Figure 4e before Au deposition. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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